REMARKS/ARGUMENTS

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

Claims 1-3, 5-10, 12-17, 19, and 20 are pending in the present application. By this response, claims 1, 5, 8, 12, 13, 15, and 19 are amended and claims 4, 11, and 18 are canceled. Claims 1, 8, and 15 are amended to incorporate the subject matter of claims 4, 11, and 18. Claims 5, 12, 13, and 19 are amended in view of the amendments to claims 1, 8, and 15 in order to provide proper antecedent basis and clarity. Reconsideration of the claims in view of the above amendments and the following remarks is respectfully requested.

I. Examiner Interview

Applicants thank Examiner Kendall for the courtesies extended to Applicants' representative during the December 20, 2006 telephone interview. During the interview, proposed amendments to claims 1, 8, and 15 were discussed. Examiner Kendall stated he would consider the proposed amendments. The substance of the interview is summarized in the remarks of sections that follow.

II. 35 U.S.C. § 102, Alleged Anticipation, Claims 1-5, 8-12, and 15-19

The Office rejects claims 1-5, 8-12, and 15-19 under 35 U.S.C. § 102 as being anticipated by Merchant et al. (US Patent No. 6,772,322 B1). This rejection is respectfully traversed.

As to claims 1, the Office Action states:

> Regarding claim 1, a method for executing instructions in a data processing system, comprising:
> associating one or more instructions of a computer program with one or more performance indicators (FIG.3, 322, see EVENT DETECTOR);
> storing the one or more performance indicators in one or more performance indicator fields of a page table (See, FIG. 5 and all associated text);
> initiating one or more counter fields in the page table for the one or more instructions in association with corresponding performance indicators of the one or more performance indicators (FIG.3, 350); and
> incrementing values in the one or more counter fields during execution of an instruction of the computer program based on whether the instruction has an associated performance indicator in a performance indicator field of the page table (FIG. 3,350 and all associated text).

Office Action dated October 6, 2006, pages 2-3.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). Applicants respectfully submit that Merchant does not teach every element of the claimed invention arranged as they are in the claims.

Amended claim 1, which is representative of the other rejected independent claims 8 and 15 with respect to similarly recited subject matter, reads as follows:

> 1. A method for executing instructions in a data processing system, comprising:
> associating one or more instructions of a computer program with one or more performance indicators;
> storing the one or more performance indicators in one or more performance indicator fields of a page table;
> initiating one or more counter fields in the page table for the one or more instructions in association with corresponding performance indicators of the one or more performance indicators;
> incrementing values in the one or more counter fields during execution of an instruction of the computer program based on whether the instruction has an associated performance indicator in a performance indicator field of the page table; and
> **storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields**. (emphasis added)

Applicants respectfully submit that Merchant does not teach every feature in amended claim 1 in the same arrangement as recited in claim 1. More specifically, Merchant does not teach storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields.

Merchant is directed to monitoring the performance of a processor. Merchant includes a performance specifier that specifies a performance data corresponding to the performance. The performance data includes an event and an instruction causing the event. Merchant provides a tag generator that is coupled to the performance specifier to generate a performance tag associated with the instruction. The performance tag is stored in a storage. Finally, Merchant provides a retirement performance monitor that is coupled to the storage to extract the performance tag when the instruction is retired.

The Office alleges that Merchant teaches storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields, in the following section:

> The tagging matrix 500 is a logical visualization of all possible combinations of events and instructions and may be useful as a design aid for performance monitor program writer. The tagging matrix 500 is essentially a map that shows the results generated by the tag generator 320 shown in FIG. 3.
>
> The event specifier 312 may be a register having M bits, each bit corresponding to an event. A performance monitor program such as the performance monitor program 131 shown in FIG. 1 may access the event specifier 312 to configure the M-bit register. The event specifier 312 may be divided into two fields, one is for internally visible events and one is for externally visible events. Internally visible events are those that can only be observed by personnel of the processor. Externally visible events are those that can be observed and accessed by users of the processor. Examples of externally visible events include cache miss, data translation look-aside buffer miss, segmentation conflict, floating point replay, memory order buffer load replay, segmentation and address translation replay, address generator unit and cache miss, data cache address and control replay, source dependency replay, misprediction, instruction tagging, and precise sampling enabling. Examples of internally visible events include writeback conflict, de-pipeline conflict, execution unit jump, control register access, and store forwarding guard.

(Merchant, column 7, lines 25-50)

In this section, Merchant describes a tagging matrix that is a logical visualization of all possible combinations of events and instructions. Merchant describes the tagging matrix as essentially a map that shows the results generated by the tag generator. Merchant further describes an event specifier as a register that has M bits, each bit corresponding to an event. The event specifier may be divided into two fields, one is for internally visible events and one is for externally visible events. Nowhere in this section, or in any other section of Merchant, is there a description of storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields. Merchant merely describes building a matrix of all possible combinations of events and instructions. One of ordinary skill in the art would know a threshold value to be a limiting value that is used to determine if another value is greater than, less than, or equal to. A matrix is merely a two dimensional array and the events and instructions are merely data. Therefore, Merchant does not teach storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields.

Thus, Merchant does not teach each and every feature of independent claims 1, 8, and 15 as is required under 35 U.S.C. § 102. At least by virtue of their dependency on independent claims 1, 8, and 15, the specific features of dependent claims 2, 3, 5, 9, 10, 12, 16, 17, and 19 are not taught by Merchant. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-3, 5, 8-10, 12, 15-17, and 19 under 35 U.S.C. § 102.

Moreover, in addition to their dependency from independent claims 1, 8, and 15, the specific features recited in dependent claims 2, 3, 5, 9, 10, 12, 16, 17, and 19 are not taught by Merchant. For

example, with regard to claims 5, 12, and 19, Merchant does not teach upon the occurrence of an event, comparing one or more values in the one or more counter fields to a threshold value in the one or more threshold fields, and generating an interrupt if a predetermined relationship between the one or more values in the one or more counter fields and the threshold value is present. The Office alleges that this feature is taught in the following sections:

> The event detector 322 receives the occurring events as generated by the event monitor circuits 210, to 210M and the specified event from the event specifier 312. The event detector 322 includes an event synchronizer 323A and an event matching logic 323B. The event synchronizer 323A synchronizes the occurring events together and with the instruction. The event matching logic 323B matches or compares the synchronized occurring event or events with the specified event or events. The event detector 322 generates an event match tag. In one embodiment, there are multiple specified events and the event detector 322 matches the specified events with multiple occurring events from the event monitor circuits 210_1 to 210_M and generates an event match tag containing match bits corresponding to matched events. If there is a match, the event detector 322 asserts the event match tag. If there is no match, the event detector 322 de-asserts the event match tag.

(Merchant, column 5, lines 28-44)

> The instruction is a micro operation and the retired instruction may be correctly or incorrectly predicted. The performance tag generates one of an interrupt and a break-point. The event is one of an externally visible event and an internally visible event. The externally visible event includes a cache miss, a data translation look-aside buffer miss, a segmentation conflict, a floating point replay, a memory order buffer load replay, a segmentation and address translation replay, an address generator unit and cache miss, a data cache address and control replay, a source dependency replay, a misprediction, an instruction tagging, and a precise sampling enabling. The internally visible event includes a writeback conflict, a de-pipeline conflict, an execution unit jump, a control register access, and a store forwarding guard. The instruction is one of a load, a store address, a store data, a micro jump, a macro jump, a transfer, a jump, a floating-point operation, a long latency integer operation, an arbitrary latency operation, a control register operation, and a fireball operation.

(Merchant, column 2, lines 33-51)

In column 5, lines 28-44, Merchant describes an event synchronizer that synchronizes occurring events together with the instruction. Merchant further describes event matching logic that matches or compares the synchronized occurring event or events with the specified event or events. Then Merchant uses and event detector to generate an event match tag. In column 2, lines 33-51, merchant describes a performance tag generating an interrupt. However, in column 5, lines 59-60, Merchant describes that a performance tag is generated by combining an event match tag to an instruction match tag. Thus, while Merchant's performance tag may generate an interrupt, the interrupt is not generated if a predetermined relationship between the one or more values in the one or more counter fields and the **threshold value** is

present, where the predefined relationship is derived by comparing one or more values in the one or more counter fields to a **threshold value** in the one or more **threshold fields**.

Therefore, in addition to being dependent on independent claims 1, 8, and 15, dependent claims 2, 3, 5, 9, 10, 12, 16, 17, and 19 are also distinguishable over Merchant by virtue of the specific features recited in these claims. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 2, 3, 5, 9, 10, 12, 16, 17, and 19 under 35 U.S.C. § 102.

Furthermore, Merchant does not teach, suggest or give any incentive to make the needed changes to reach the presently claimed invention. Absent the Office pointing out some teaching or incentive to implement Merchant such that one or more threshold values are stored in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields, one of ordinary skill in the art would not be led to modify Merchant to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion or incentive to modify merchant in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

III. 35 U.S.C. § 103, Alleged Obviousness, Claims 6, 7, 13, 14, and 20

The Office rejects claims 6, 7, 13, 14, and 20 under 35 U.S.C. § 103 as being unpatentable over Merchant et al. (US Patent No. 6,772,322 B1) in view of Roth et al. (US Patent No. 5,937,437). This rejection is respectfully traversed.

Claims 6, 7, 13, 14, and 20 are dependent on independent claims 1, 8, and 15 and, thus, these claims distinguish over Merchant for at least the reasons noted above with regard to claims 1, 8, and 15. Moreover, Roth does not provide for the deficiencies of Merchant and, thus, any alleged combination of Merchant and Roth would not be sufficient to reject independent claims 1, 8, and 15 or claims 6, 7, 13, 14, and 20 by virtue of their dependency. That is, Roth does not teach or suggest storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields.

Moreover, neither Merchant nor Roth teaches or suggests the desirability of incorporating the subject matter of the other when these cited references are considered as a whole by one of ordinary skill in the art. That is, there is no motivation offered in either reference for the alleged combination. The Office alleges that the motivation for the combination is "because, it would enable verifying cache hits." As discussed above, Merchant fails to teach storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or

more counter fields. While Roth may describe a relationship between real addresses and virtual addresses, Roth does not teach or suggest storing one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields. Thus, the only teaching or suggestion to even attempt the alleged combination is based on a prior knowledge of Applicants' claimed invention thereby constituting impermissible hindsight reconstruction using Applicants' own disclosure as a guide.

One of ordinary skill in the art, being presented only with Merchant and Roth, and without having a prior knowledge of Applicants' claimed invention, would not have found it obvious to combine and modify Merchant and Roth to arrive at Applicants' claimed invention. To the contrary, even if one were somehow motivated to combine Merchant and Roth, and it were somehow possible to combine the two systems, the result would not be the invention, as recited in claims 1, 8, and 15. That is, the resulting system still would not store one or more threshold values in one or more threshold fields of the page table in association with the one or more performance indicator fields and the one or more counter fields.

Thus, in view of the above, Merchant and Roth, taken either alone or in combination, fail to teach or suggest the specific features recited in independent claims 1, 8, and 15, from which claims 6, 7, 13, 14, and 20 depend. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 6, 7, 13, 14, and 20 under 35 U.S.C. § 103.

IV. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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